FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

ATTY. DOCKET NO.	SERIAL NO.
00174/188	09/761,609
APPLICANT: Andy L. Lee et al.	
FILING DATE: 1/16/01	GROUP: 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
HLC	5,212,652	5/18/93	Agrawal et al.	364	489	
	5,343,406	8/30/94	Freeman et al.	364	490	
	5,352,940	10/4/94	Watson	307	465	
	5,414,377	5/9/95	Freidin	326	41	
	5,432,719	7/11/95	Freeman et al.	364	579	
	5,488,316	1/30/96	Freeman et al.	326	41	
	5,550,782	8/27/96	Cliff et al.	365	230.03	
	5,566,123	10/15/96	Freidin et al.	365	230.05	
	5,572,148	11/5/96	Lytle et al.	326	41	
	5,631,577	5/20/97	Freidin et al.	326	40	
	5,648,732	7/15/97	Duncan	326	40	
	5,689,195	11/18/97	Cliff et al.	326	41	
	5,758,192	5/26/98	Alfke	395	877	
	5,889,413	3/30/99	Bauer	326	40	
	5,898,893	4/27/99	Alfke	395	877	
	5,926,036	7/20/99	Cliff et al.	326	40	
HLC	6,049,223	4/11/00	Lytle et al.	326	40	
HLC	U.S. Patent Appln. No. 09/007,718		Zaveri et al.			1/15/98
HLC	U.S. Patent Appln. No. 09/266,235		Jefferson et al.			3/10/99

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

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EXAMINER INITIAL	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)
HK	P. Chow et al., "A 1.2μm CMOS FPGA using Cascaded Logic Blocks and Segmented Routing", FPGAs, Chapter 3.2, pp. 91-102, W.R. Moore and W. Luk (eds.), Abingdon EE&CS Books, Abingdon, (UK), 1991.
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	"Optimized Reconfigurable Cell Array (ORCA) Series Field-Programmable Gate Arrays", Advance Data Sheet, AT&T Microelectronics, February 1993, pp. 1-36 and 65-87.
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	B. Klein, "Use LFSRs to Build Fast FPGA-Based Counters", Electronic Design, March 21, 1994, pp. 87, 88, 90, 94, 96, 97, and 100,
	A. DeHon, "Reconfigurable Architectures for General-Purpose Computing", M.I.T. Ph.D. thesis, September 1996.
	R. Iwanczuk, "Using the XC4000 RAM Capability", XAPP 031.000, Xilinx, Inc., San Jose, CA.
	J.R. Hauser et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor", 0-8186-8159-4/97 $10.00 © 1997 IEEE, pp. 12-21.
	A. Ohta et al., "New FPGA Architecture for Bit-Serial Pipeline Datapath", 0-8186-8900-5/98 $10.00 © 1998 IEEE, pp. 58-67.
	"XC4000E and XC4000X Series Field Programmable Gate Arrays; Product Specification", May 14, 1999 (Version 1.6), Xilinx Inc., San Jose, CA, pp. 6-5 through 6-72.
	"Flex 10K Embedded Programmable Logic Family", Data Sheet, June 1999, ver. 4.01, Altera Corporation, San Jose, CA, pp. 1-137.
	"Flex 10KE Embedded Programmable Logic Family", Data Sheet, August 1999, ver. 2.02, Altera Corporation, San Jose, CA, pp, 1-120.
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HK	"Triscend E5 Configurable System-on-Chip Family", Triscend Corporation, January 2000 (Version 1.00) Product Description, cover page and pp. 25-28.

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HC	"Apex 20K Programmable Logic Device Family", Data Sheet, March 2000, ver. 2.06, Altera Corporation, San Jose, CA, pp. 1-208.
HK	"Virtex 2.5V Field Programmable Gate Arrays", DS003 (v. 2.0), Preliminary Product Specification, March 9, 2000, Xilinx, Inc., San Jose, CA, pp. 1-72.
HC	"Virtex™-E 1.8V Extended Memory Field Programmable Gate Arrays", DS025 (v1.0) March 23, 2000, Advance Product Specification, Xilinx Inc., San Jose, CA, pp. 1 and 6.

H. Kim

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